What is claimed is:

[Claim 1] 1. A power clamp for an integrated circuit, comprising:

a transistor network connected between a voltage source and a ground;

a bias network configured to bias a gate of a first transistor of the transistor network to a portion of a voltage value of the voltage source; and

a trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of a second transistor of the transistor network.

[Claim 2] 2. The power clamp of claim 1, wherein the transistor network comprises a first nFET and a second nFET connected in series with one another between the voltage source and a ground.

[Claim 3] 3. The power clamp of claim 2, wherein the transistor network further comprises a third nFET connected in series with the first nFET and the second nFET between the voltage source and the ground.

[Claim 4] 4 The power clamp of claim 3, wherein the bias network further comprises a voltage divider configured to communicate a portion of the voltage from the voltage source to the gate of the first transistor and a gate of the third nFET.

[Claim 5] 5. The power clamp of claim 1, wherein the bias network comprises a voltage divider configured to communicate a portion of the voltage from the voltage source to the gate of the first transistor.

[Claim 6] 6. The power clamp of claim 1, wherein the trigger network comprises a resistor and a capacitor configured to filter out non-electrostatic discharge events from the gate of the second transistor.

[Claim 7] 7. A power clamp for an integrated circuit, comprising:

at least an upper and a lower nFET connected in series with one another between a pair of power supply rails;

a voltage divider configured to bias a gate of the upper nFET to a prescribed value; and

a low frequency filter connected to a gate of the lower nFET and configured to filter out low frequency signals between at least one power supply rail and the gate of the lower nFET.

[Claim 8] 8. The power clamp of claim 7, wherein the gate of the upper nFET is biased to a prescribed fraction of a voltage between the pair of power supply rails.

[Claim 9] 9. The power clamp of claim 7, wherein the voltage divider is connected between the pair of power supply rails and comprises a high impedance therebetween.

[Claim 10] 10. The power clamp of claim 9, wherein the voltage divider comprises at least one resistor.

[Claim 11] 11. The power clamp of claim 7, wherein the low frequency filter communicates with a source and a drain of the lower nFET.

[Claim 12] 12. A method of protecting against electrostatic discharge, comprising:

configuring a gate of at least one upper transistor of a transistor network connected between power rails to be biased to a prescribed value; and

coupling an electrostatic discharge event to a gate of a lower transistor of the transistor network.

[Claim 13] 13. The method of claim 12, further comprising biasing the gate of the at least one upper transistor with a voltage divider connected between the power rails.

[Claim 14] 14. The method of claim 12, further comprising configuring the voltage divider to comprise a high impedance.

[Claim 15] 15. The method of claim 14, further comprising biasing the gate of the at least one upper transistor to a prescribed fraction of the voltage of at least one power rail of the power rails.

[Claim 16] 16. The method of claim 12, wherein configuring a gate of at least one upper transistor of a transistor network connected between power rails to be biased to a prescribed value comprises applying a voltage to at least one power rail of the power rails.

[Claim 17] 17. The method of claim 12, wherein configuring a gate of at least one upper transistor of a transistor network connected between power rails to be biased to a prescribed value comprises attaching a bias network between at least one power rail of the power rails and the transistor network.

[Claim 18] 18. The method of claim 12, further comprising coupling an electrostatic discharge event to a gate of a lower transistor with a high pass filter.

[Claim 19] 19. The method of claim 18, further comprising configuring the high pass filter to comprise a time constant of about one microsecond.

[Claim 20] 20. The method of claim 12, further comprising configuring at least one power rail of the power rails to be in electrical communication with a voltage source, and configuring at least one power rail of the power rails to be in electrical communication with ground.